

FIG. 2

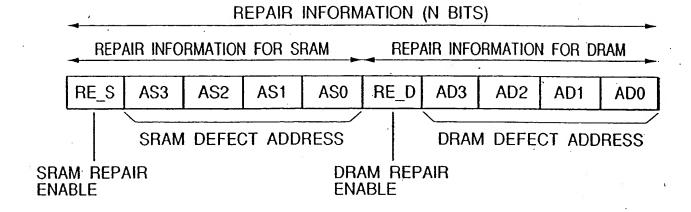
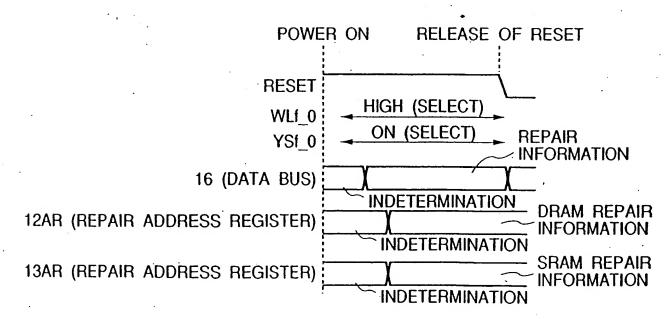
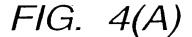


FIG. 3





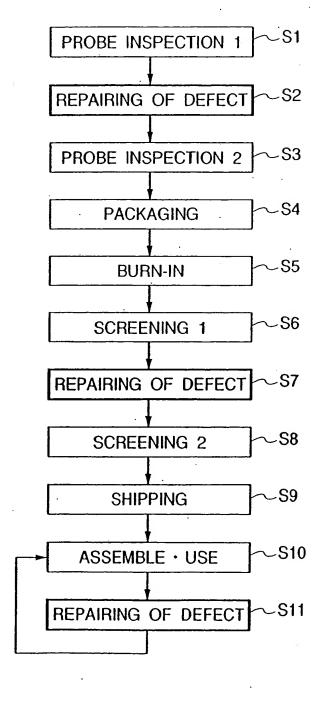


FIG. 4(B)

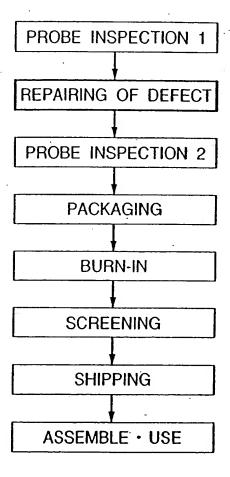


FIG. 5

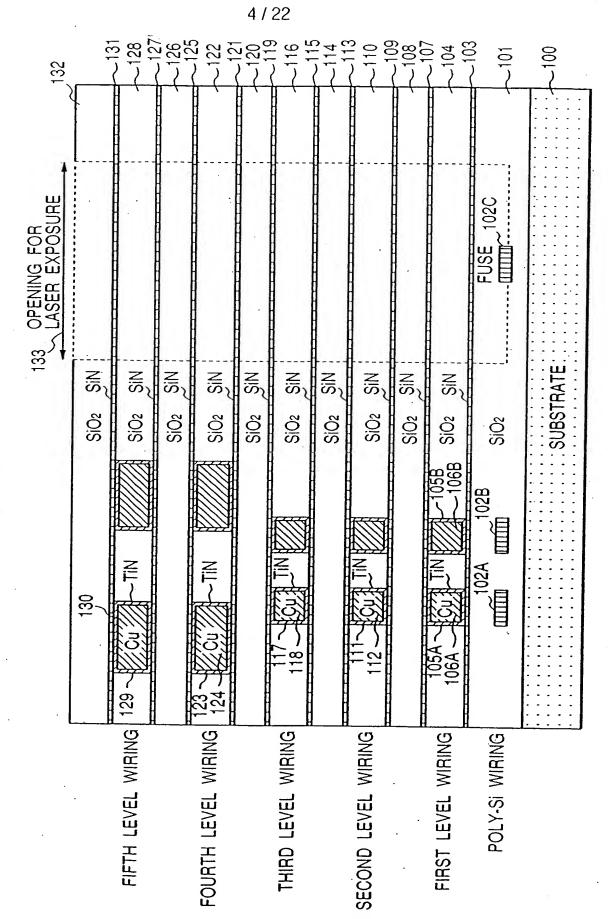


FIG. 6

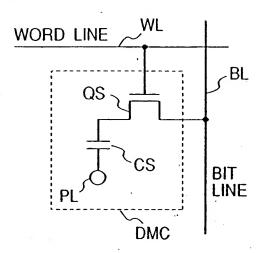


FIG. 8

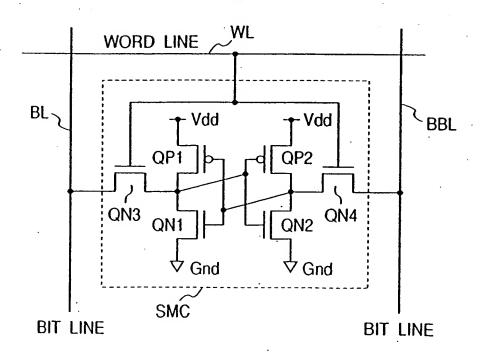
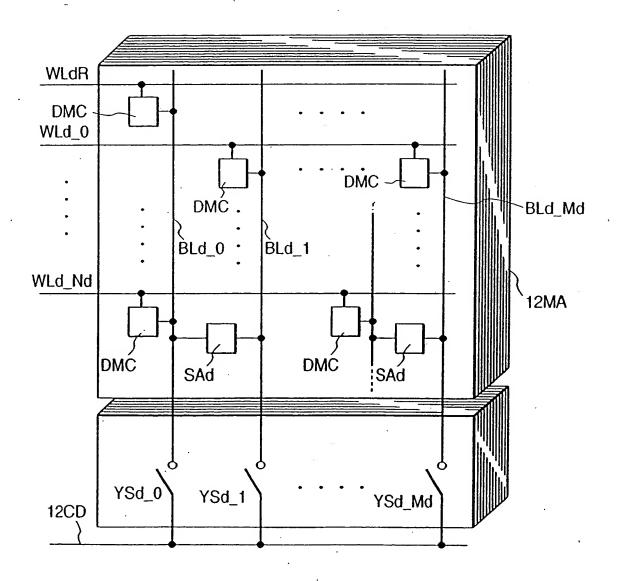


FIG. 7



 $(\overline{})$

FIG. 9

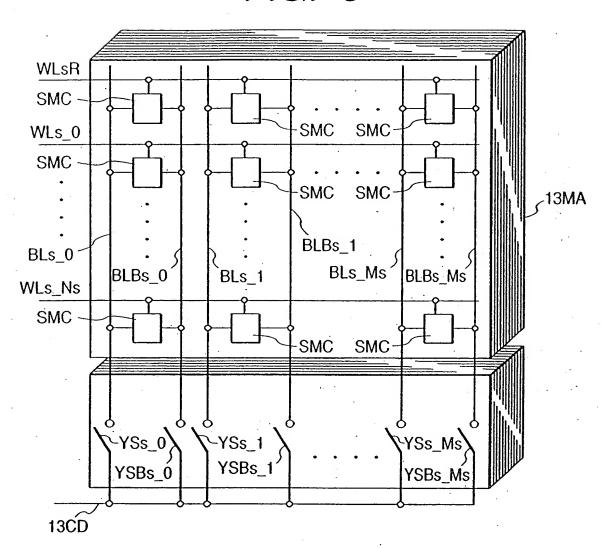


FIG. 10

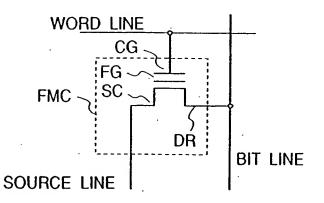


FIG. 11

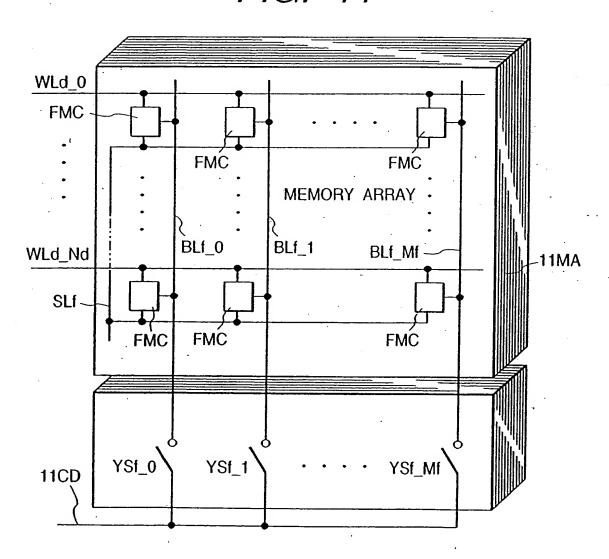


FIG. 12

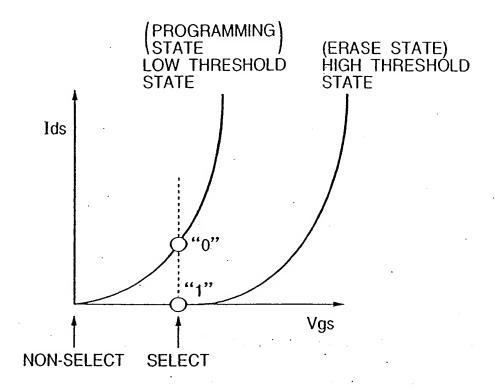
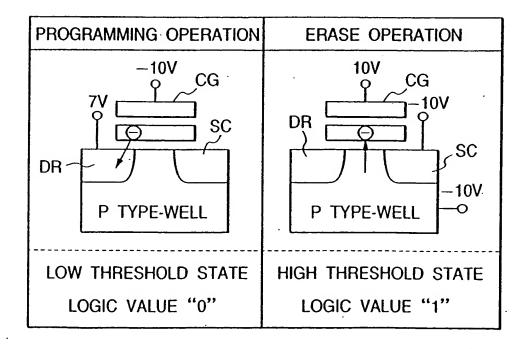


FIG. 13



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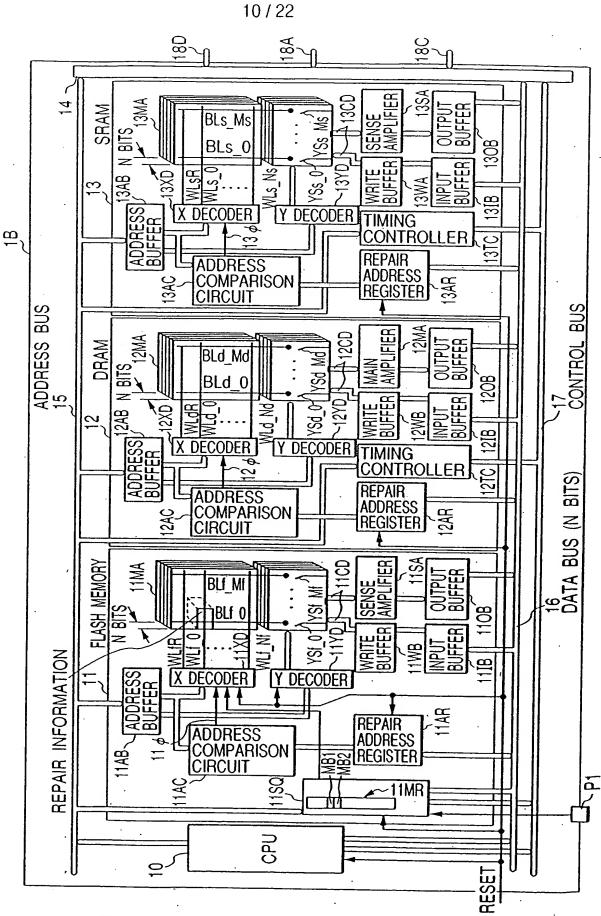


FIG. 15

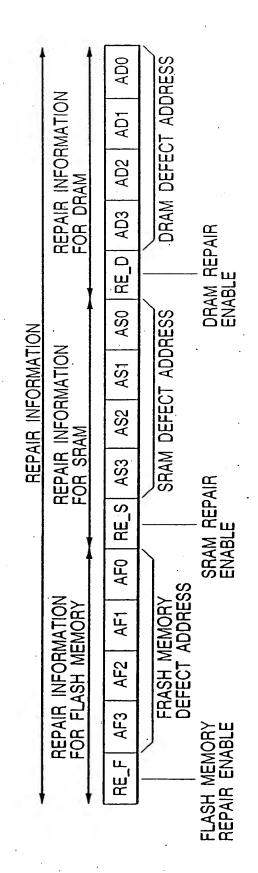
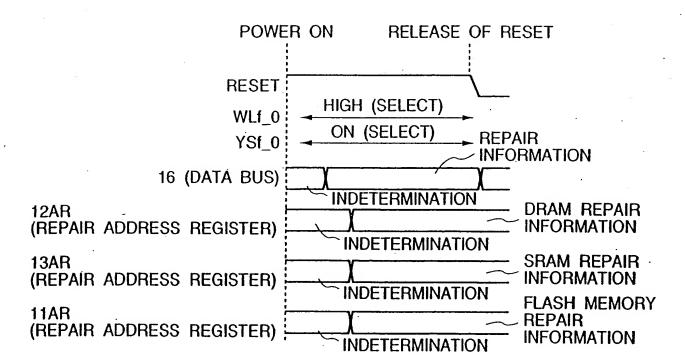


FIG. 16

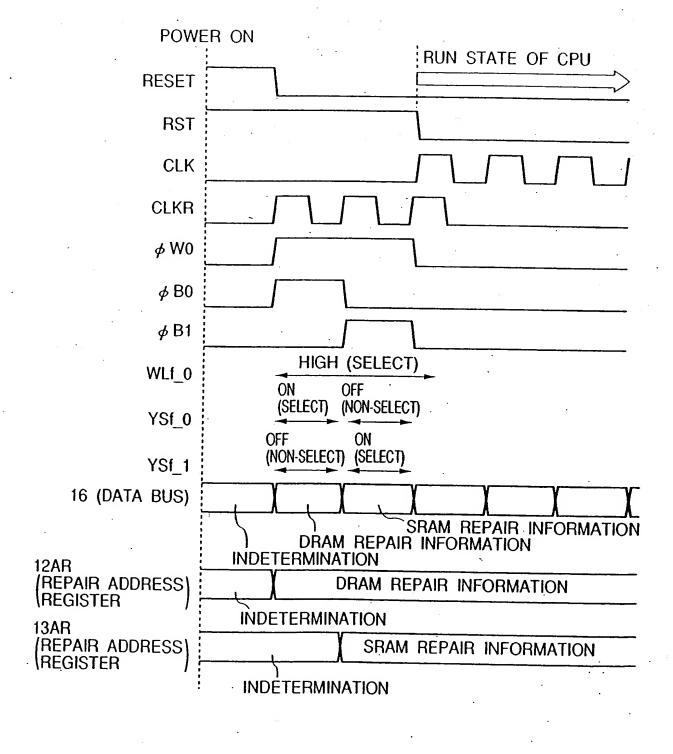


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F/G. 1

FIG. 18



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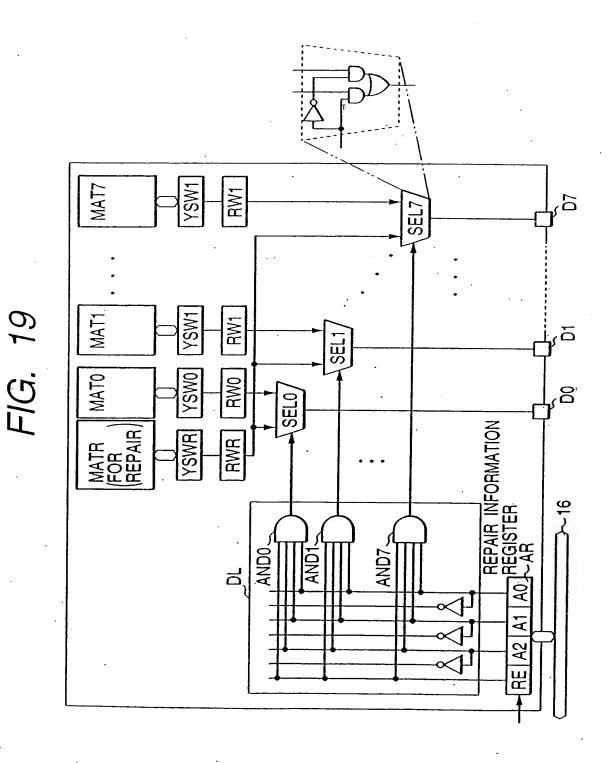


FIG. 20

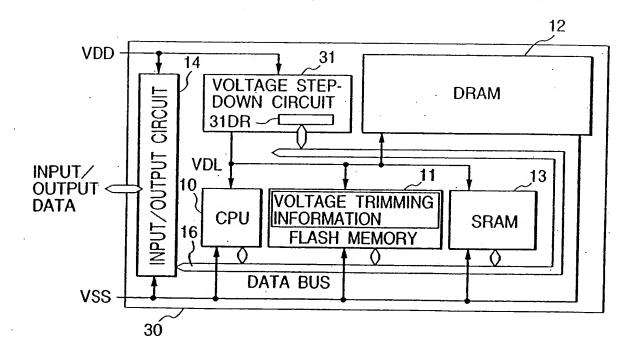
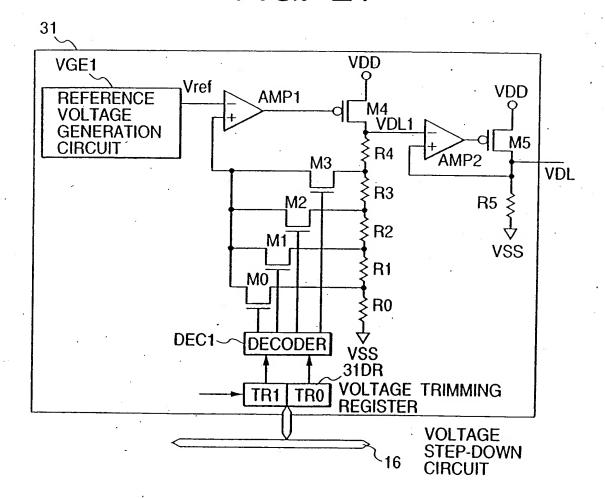


FIG. 21



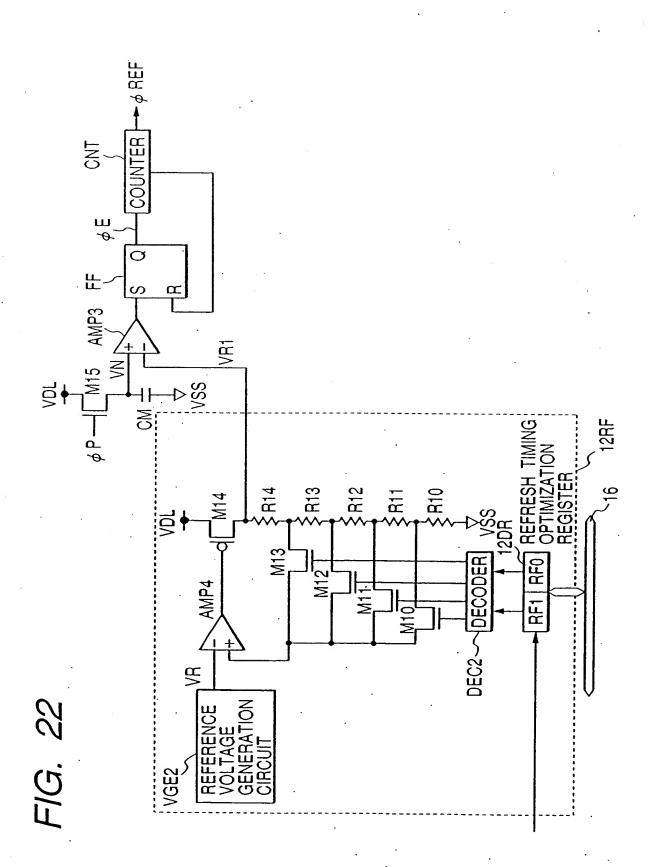
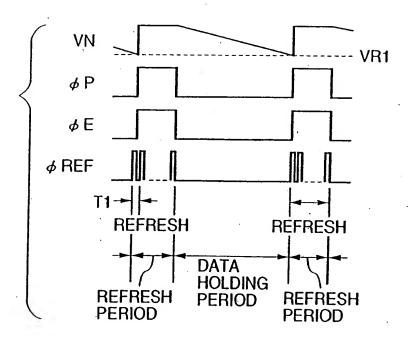


FIG. 23



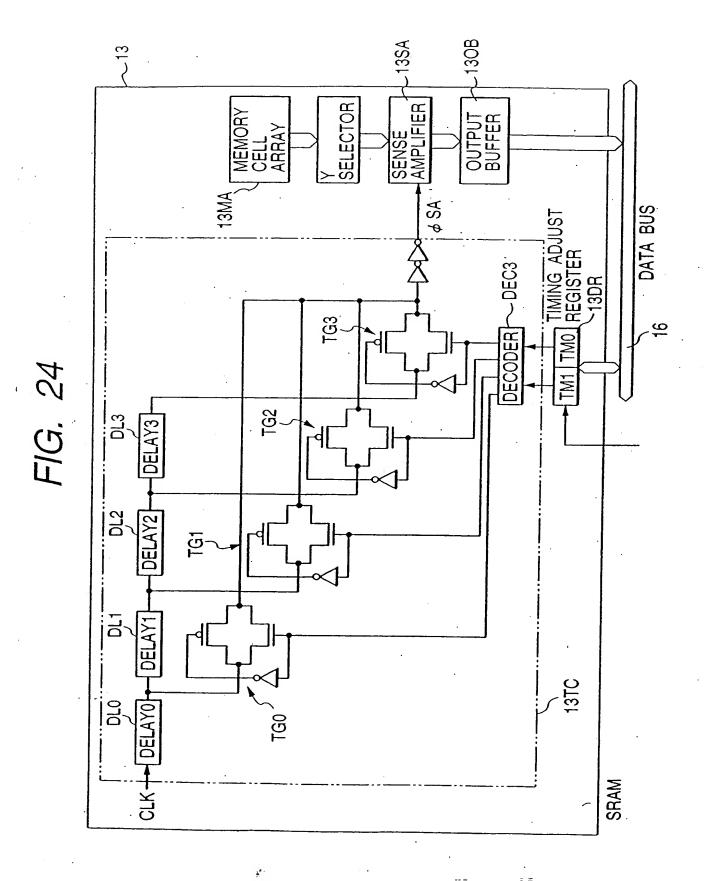


FIG. 25

TM1|TM0|RF1|RF0|TR1|TR0|RE_F|AF3|AF2|AF1|AF0|RE_S|AS3|AS2|AS1|AS0|RE_D|AD3|AD2|AD1|AD0 REPAIR INFORMATION FOR DRAM DRAM DEFECT ADDRESS DRAM REPAIR ENABLE SRAM DEFECT ADDRESS REPAIR INFORMATION FOR SRAM REPAIR INFORMATION SRAM REPAIR ENABLE FRASH MEMORY DEFECT ADDRESS REPAIR INFORMATION FOR FLASH MEMORY **NFORMATION** STEP-DOWN CIRCUIT VOLTAGE TIMMING DRAM REFRESH TIMING OPTIMIZATION INFORMATION SRAM TIMING ADJUSTMENT INFORMATION

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FIG. 26

